# Single N-Channel Enhancement Mode MOSFET

$V_{DS}$=60V, $I_D$=60A, $R_{DS(ON)}$=11.5 mΩ

## DESCRIPTION

The OR7060 is N-Channel logic enhancement mode power field effect transistors designed for high current switching applications.

Rugged $E_{AS}$ capability and ultra low $R_{DS(ON)}$ is suitable for PWM, load switching especially for E-Bike controller applications.

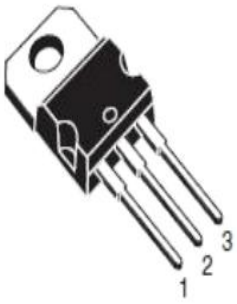
## FEATURE

- 60V/60A: $R_{DS(ON)}$<15mΩ@$V_{GS}$=10V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Special designed for E-bike controller
- Full RoHS compliance
- TO-220 package design

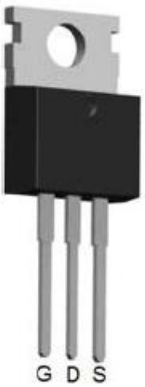
## APPLICATIONS

- 48V E-bike controller applications
- Hard switched and high frequency circuits
- Uninterruptible power supply

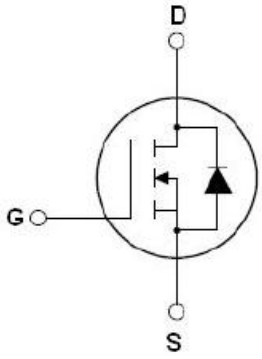
## PIN CONFIGURATION




TO-220




To-220 Top View




Schematic Diagram

## ■ ABSOLUTE MAXIMUM RATINGS ($T_A$=25°C Unless otherwise noted)

| Symbol | Parameter | | Typical | Unit |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 60 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±25 | V |
| $I_D$ | Continuous Drain Current($T_J$=150°C) | $V_{GS}$=-10V | 60 | A |
| $I_{DM}$ | Pulsed Drain Current | | 180 | A |
| $T_J$ | Operation Junction Temperature | | -55~150 | °C |
| $T_{STG}$ | Storage Temperature Range | | -55~150 | °C |
| $P_D$ | Power Dissipation($T_C$=25 °C) | | 68 | W |
| $E_{AS}$ | Single Pulse Avalanche Energy ($T_J$=25 °C,$V_{DD}$=40V,$V_{GS}$=10V, $R_G$=25Ω) | | 506 | mJ |
| $R_{\theta JC}$ | Thermal Resistance-Junction to Ambient | | 1.25 | °C/W |

Note: Absolute maxinum ratings are those values beyoud which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## ■ ELECTRICAL CHARACTERISTICS ($T_A$=25°C Unless otherwise noted)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Static Parameters | | | | | | |
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V, $I_{DS}$=250μA | 60 | - | - | V |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$= $V_{CS}$, $I_{DS}$=250μA | 2 | - | 4 | V |
| $I_{GSS}$ | Gate Leakage Current | $V_{DS}$=0V, $V_{GS}$ =±20V | - | - | ±100 | nA |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=60V, $V_{GS}$ =0V $T_C$=25 °C | - | - | 1 | μA |
| | | $V_{DS}$=60V, $V_{GS}$ =0V $T_C$=125 °C | - | - | 10 | μA |
| $R_{DS(ON)}$ | Drain-Source On-Resistance | $V_{GS}$= 10V, $I_{DS}$=40A | - | 11.5 | 15 | mΩ |
| Source-Drain Diode | | | | | | |
| $I_S$ | Diode Forward Current (Max.) | | - | 60 | - | A |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=40A,$V_{GS}$=0V | | 0.85 | 0.99 | V |
| Dynamic Parameters | | | | | | |
| $Q_g$ | Total Gate Charge | $V_{DS}$=30V, $V_{GS}$ =10V $I_D$=15A | - | 50 | - | nC |
| $Q_{gs}$ | Gate-Source Charge | | - | 12 | - | |

| | | | | | | |
|---|---|---|---|---|---|---|
| $Q_{gd}$ | Gate-Drain Charge | | - | 23 | - | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$=25V, $V_{GS}$ =0V F=1MHz | - | 1717 | - | pF |
| $C_{oss}$ | Output Capacitance | | - | 180 | - | |
| $C_{rss}$ | Reverse Transfer Capacitance | | - | 140 | - | |
| $t_{d(on)}$ | Turn-On Time | $V_{DS}$=30V, $R_L$=2.5Ω $V_{GS}$=10V, $R_G$=3Ω | - | 15 | - | nS |
| $t_r$ | | | - | 25 | - | |
| $t_{d(off)}$ | Turn-Off Time | | - | 50 | - | |
| $t_f$ | | | - | 23 | - | |

Note: 1. Pulse test: pulse width≤300us, duty cycle≤2%;

2. Static parameters are based on package level with recommened wire-bonding

## ■ *TYPICAL CHARACTERISTICS (TA=25°C Unless otherwise noted)*

Figure1. Output Characteristics

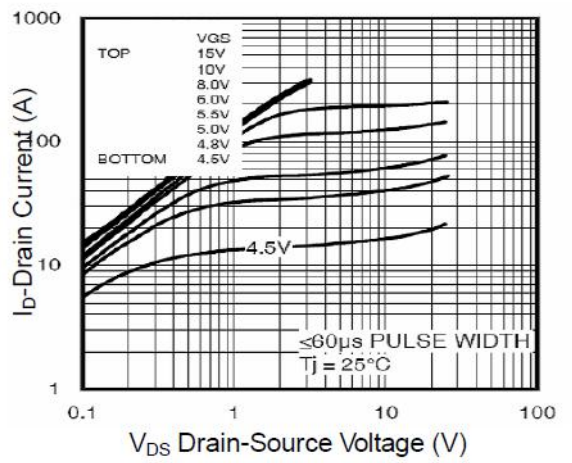



Figure2. Transfer Characteristics

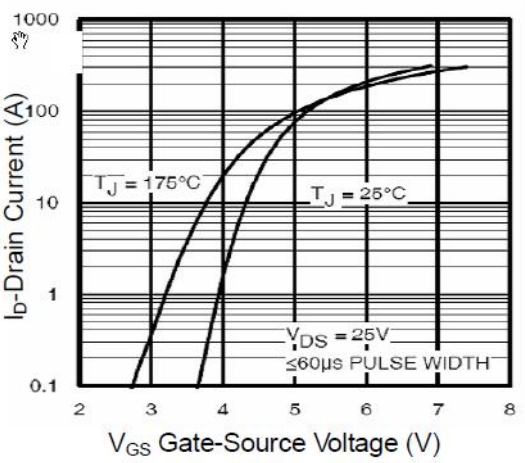



Figure3. BVDSS vs Junction Temperature

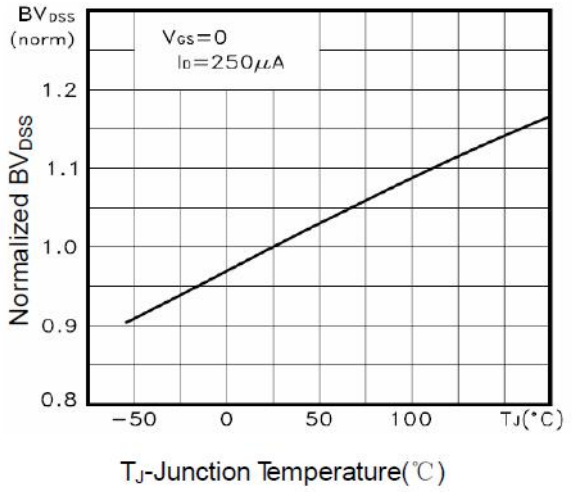



Figure4. ID vs Junction Temperature

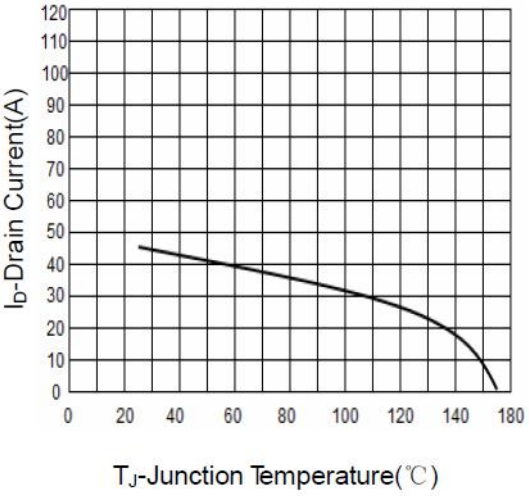



Figure5. VGS(th) vs Junction Temperature

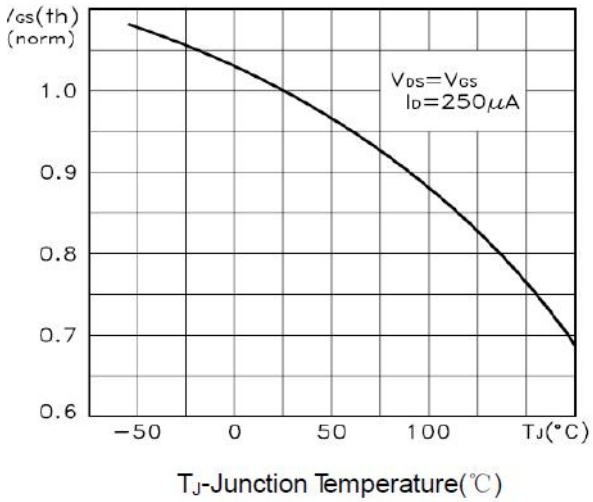
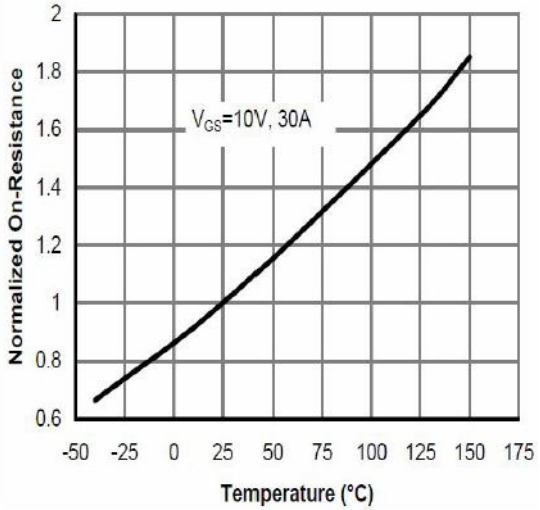



Figure6. Rdson Vs Junction Temperature




## ■ *TYPICAL CHARACTERISTICS (TA=25°C Unless otherwise noted) （Continue）*

**Figure7. Gate Charge**

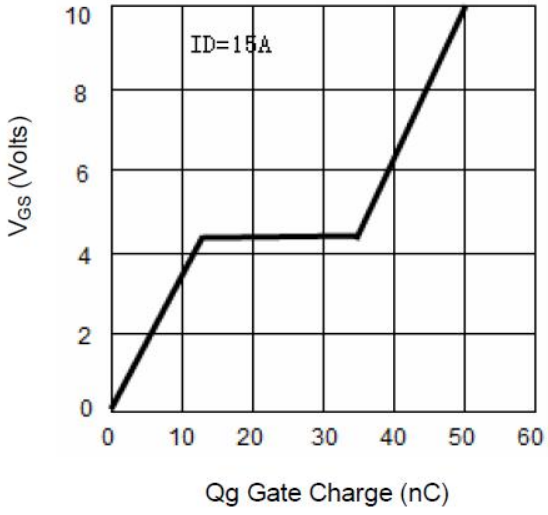



**Figure8. Capacitance vs Vds**

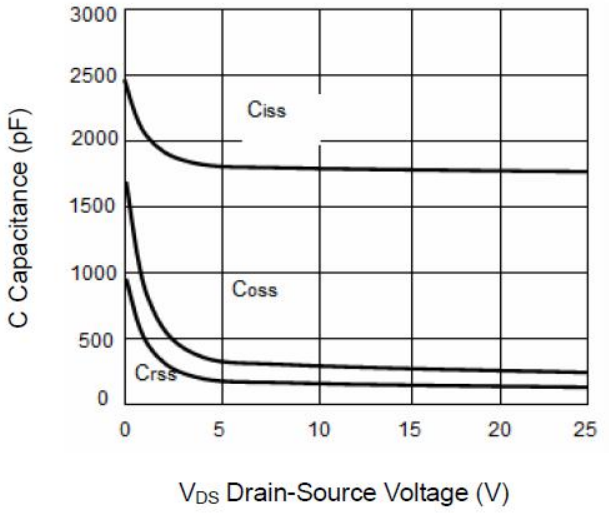



**Figure9. Source- Drain Diode Forward**

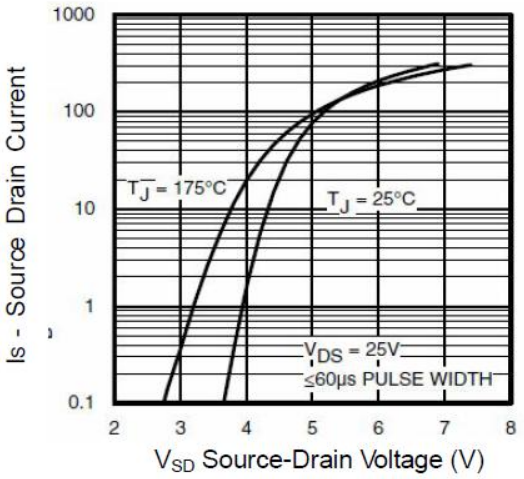



**Figure10. Safe Operation Area**

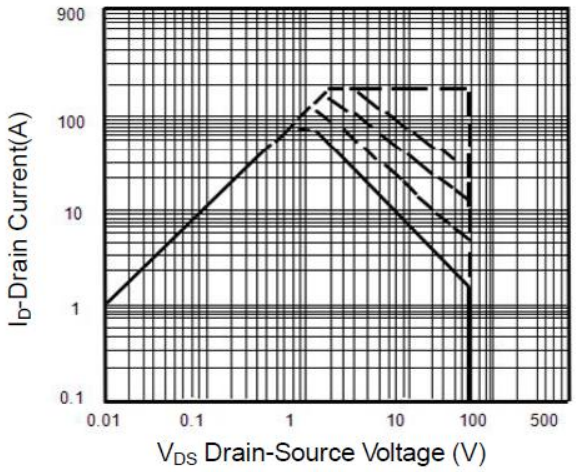
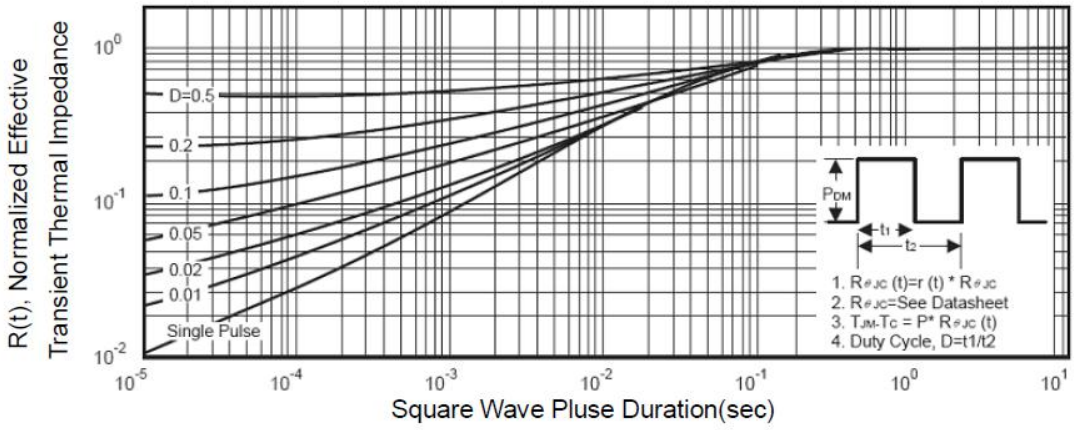
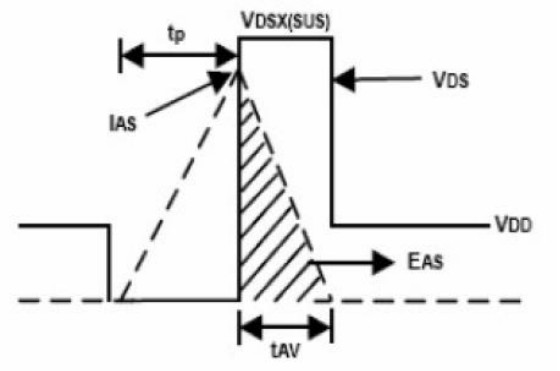
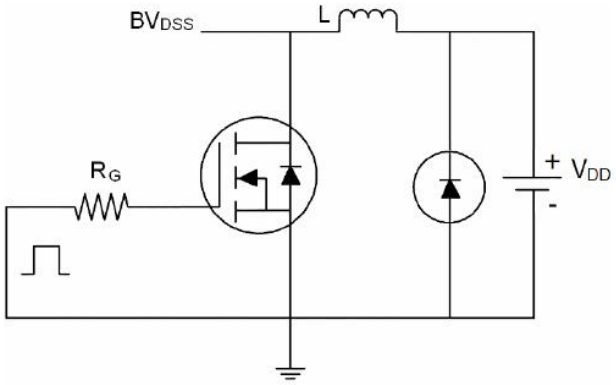



**Figure11. Normalized Maximum Transient Thermal Impedance**

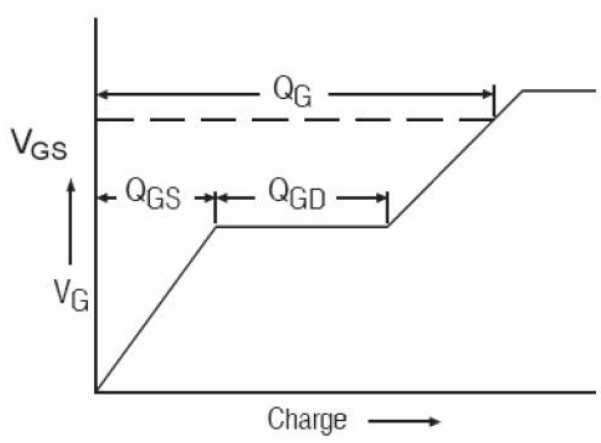


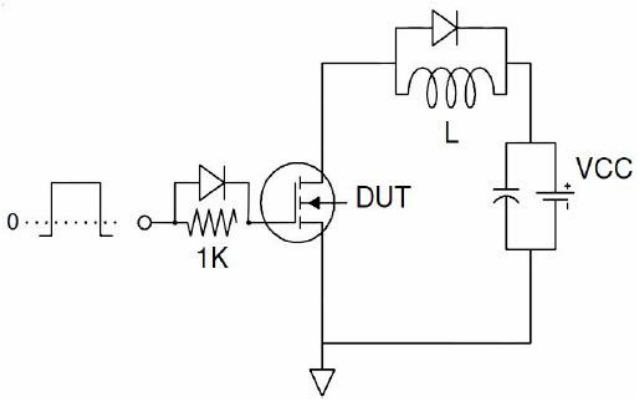
1) $E_{AS}$ Test Circuits



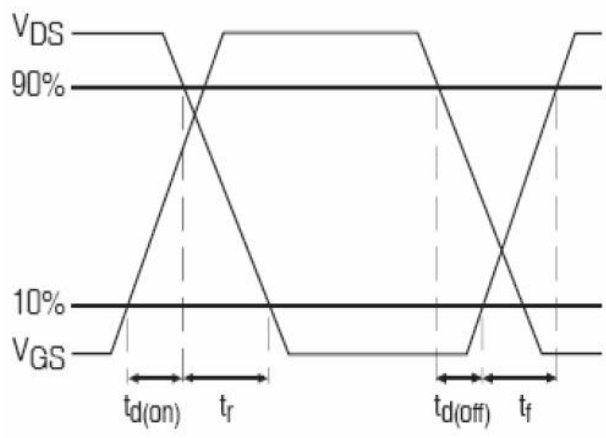



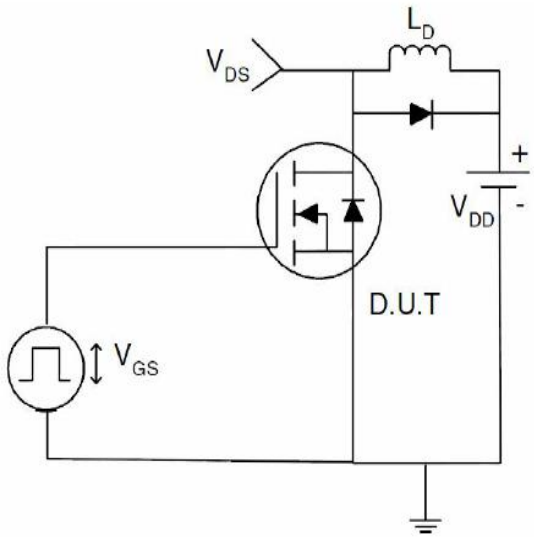

2) Gate Charge Test Circuit:



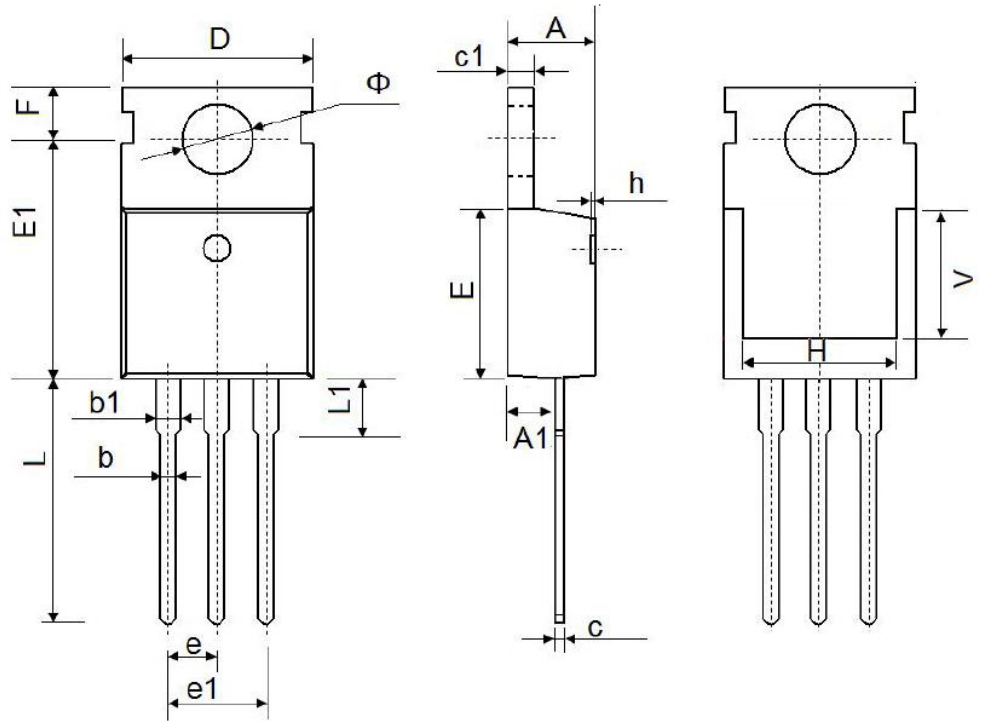




3) Switch Time Test Circuit:




## ■ *T0-220 PACKAGE DIMENSIONS*




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max |
| A | 4.400 | 4.600 | 0.173 | 0.181 |
| A1 | 2.250 | 2.550 | 0.089 | 0.100 |
| b | 0.710 | 0.910 | 0.028 | 0.036 |
| b1 | 1.170 | 1.370 | 0.046 | 0.054 |
| c | 0.330 | 0.650 | 0.013 | 0.026 |
| c1 | 1.200 | 1.400 | 0.047 | 0.055 |
| D | 9.910 | 10.250 | 0.390 | 0.404 |
| E | 8.9500 | 9.750 | 0.352 | 0.384 |
| E1 | 12.650 | 12.950 | 0.498 | 0.510 |
| e | 2.540 TYP. | | 0.100TYP. | |
| e1 | 4.980 | 5.180 | 0.196 | 0.204 |
| F | 2.650 | 2.950 | 0.104 | 0.116 |
| H | 7.900 | 8.100 | 0.311 | 0.319 |
| h | 0.000 | 0.300 | 0.000 | 0.012 |
| L | 12.900 | 13.400 | 0.508 | 0.528 |
| L1 | 2.850 | 3.250 | 0.112 | 0.128 |
| V | 7.500 REF. | | 0.295 REF. | |
| Φ | 3.400 | 3.800 | 0.134 | 0.150 |